Curriculum Vitae

Lan-Da Van (范倫達)

Title	Professor
Birthday	Oct. 09, 1972.
Society	ACM Member, HEA Fellow, IEEE Senior Member
School Name	National Yang Ming Chiao Tung University[*1]
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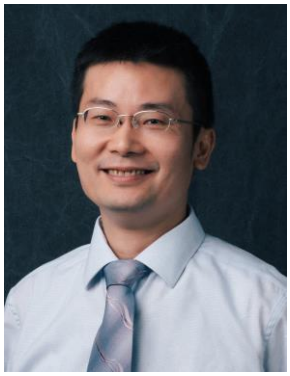
URL	http://people.cs.nctu.edu.tw/~ldvan/
Publication-URL	http://viplab.cs.nctu.edu.tw/publications.php
Google Citations	https://scholar.google.com.tw/citations?user=qbTpOVsAAAAJ&hl=zh-TW&oi=ao



*1: The merger of National Yang-Ming University and National Chiao Tung University on February 01, 2021.

Education

Ph.D., Electrical Engineering, National Taiwan University, Taiwan. (1997/09 ~ 2001/06)
M.S., Electrical Engineering, Tatung Institute of Technology[*2], Taiwan. (1995/09 ~ 1997/06)
B.S. (Honors), Dept. of Electrical Engineering, Tatung Institute of Technology[*2], Taiwan. (1991/09 ~ 1995/06)

*2: Tatung Institute of Technology has renamed as Tatung University in 1999, Taipei, Taiwan.

Experience

Associate Chief Director, Microelectronics and Information Research Center (MIRC), National Yang Ming Chiao Tung University, Taiwan. (First Level Research Center) [Chinese: 國立陽明交通大學-電子與資訊研究中心: 副中心主任] (2021/05 ~ Present)
Professor, Department of Computer Science, National Yang Ming Chiao Tung University, Taiwan. (2021/02 ~ Present)
Professor, Department of Computer Science, National Chiao Tung University, Taiwan. (2020/08 ~ 2021/01)
Associate Professor, Department of Computer Science, National Chiao Tung University, Taiwan. (2011/08 ~ 2020/07)
Assistant Professor, Department of Computer Science, National Chiao Tung University, Taiwan. (2006/02 ~ 2011/07)
Joint Appointment Professor, Industry Academia Innovation School, National Yang Ming Chiao Tung University, Taiwan. (2022/02 ~ 2024/07)
Joint Appointment Professor, College of Artificial Intelligence, National Yang Ming Chiao Tung University, Taiwan. (2021/02 ~ 2021/07)
Joint Appointment Professor, College of Artificial Intelligence, National Chiao Tung University, Taiwan. (2020/08 ~ 2021/01)
Joint Appointment Associate Professor, College of Artificial Intelligence, National Chiao Tung University, Taiwan. (2019/08 ~ 2020/07)
Director, M2M/IoT R&D Center, National Yang Ming Chiao Tung University, Taiwan. (College Level Research Center) (2021/06 ~ 2024/06)
Associate Director, M2M/IoT R&D Center, National Yang Ming Chiao Tung University, Taiwan. (College Level Research Center) (2018/06 ~ 2021/06)
Director, Software/Hardware System Integration Laboratory, National Yang Ming Chiao Tung University, Taiwan. (Department Level Laboratory) (2019/08 ~ Present)
Adjunct Research Fellow, Taiwan Semiconductor Research Institute (TSRI), National Applied

Research Laboratories (NARL), Taiwan. (2021/01 ~ 2022/12)
Deputy Department Manager, National Chip Implementation Center (CIC), Taiwan. (2004/02 ~ 2006/01)
Associate Researcher, National Chip Implementation Center (CIC), Taiwan. (2001/10 ~ 2006/01)

Research Field

Intelligent/VLSI algorithms, architectures, chips, systems, and applications for digital signal processing and adaptive/machine leaning computation. Specifically, the designs of low-power/high-performance/ cost-effective adaptive filter, computer arithmetic, independent component analysis (ICA), multi-dimensional filter, transform, 3-D graphics system, intelligent elevator system, and UAV and wearable data fusion system.

Activity

1) Associate Editor/Guest Editor

- Associate Editor, IEEE Transactions on Emerging Topics in Computing. (JCR IF=7.691, 2022/01 ~ Present)
- Associate Editor, ACM Computing Surveys. (JCR IF=10.282, 2020/01 ~ Present)
- Associate Editor, IEEE Access. (JCR IF=3.367, 2018/02 ~ 2022/01)
- Associate Editor, IEEE Transactions on Computers. (JCR IF=2.663, 2014/10 ~ 2018/12)
- Member, Multimedia Team at the IEEE Transactions on Computers Editorial Board (MTTC). (2015/12 ~ 2018/12, http://staff.polito.it/paolo.montuschi/news-from-EIC-TC.html)
- Board Member, Journal of Medical Imaging and Health Informatics. (JCR IF=0.659, 2017/08 ~ 2021/12)
- Associate Editor, Journal of Medical Imaging and Health Informatics. (2014/10 ~ 2017/08)
- Guest Editor, Journal of Medical Imaging and Health Informatics. (Special Issue on April 2015, with Prof. Zhiguo Zhang)
  Special Issue Title: Advanced Signal Processing Technologies and Systems for Healthcare Applications

2) Advisory/Steering Committee Member

- International Steering Committee Member, IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2021.

3) Organizing Committee Member

- Technical Program Committee Co-Chair, International SoC Design Conference (ISOCC), 2022.
- Special Session Co-Chair, IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), 2022.
- Special Session Co-Chair, International SoC Design Conference (ISOCC), 2021.
- Tutorial Co-Chair, IEEE International System-on-Chip Conference (SOCC), 2021.
- Special Session Co-Chair, IEEE International Symposium on Circuits and Systems (ISCAS), 2021.
- Technical Program Committee Co-Chair, IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2020.
- Tutorial Co-Chair, IEEE International System-on-Chip Conference (SOCC), 2020.
- Publicity Co-Chair, IEEE International System-on-Chip Conference (SOCC), 2019.
- Special Session Co-Chair, IEEE International Conference on Digital Signal Processing (DSP), 2018.
- Program Co-Chair, NCTU Forum of Technology and Application of Internet of Things, 2016.
- Officer, IEEE Taipei Section. (2009~2010)
- Chairman, IEEE National Taiwan University (NTU) Student Branch, 2000.

4) Technical/Program/Review Committee (TC/PC/TPC/RC) Member

- VLSI Systems and Applications TC Member, IEEE Circuits and Systems Society. (2010 ~ 2021)
- Circuits and Systems for Communications TC Member, IEEE Circuits and Systems Society.

(2010 ~ 2021)

- Nanoelectronics and Gigascale Systems TC Member, IEEE Circuits and Systems Society. (2008 ~ 2021)
- Track Chair, IEEE 14th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC) ("Algorithms, Architecture and Hardware for AI" track, 2021).
- TPC Member, IEEE Nordic Circuits and Systems Conference (NORCAS), 2021.
- PC Member, ACM International Conference on Multimedia Retrieval (ICMR), 2021.
- Review Committee Member, IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), 2021.
- TPC Member, IEEE Circuits and Systems Society in Latin America (LASCAS), 2021.
- TPC Member, IEEE International Conference on Internet of Things and Intelligence Application, 2020.
- TPC Member, IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2020.
- TPC Member, IEEE Nordic Circuits and Systems Conference (NORCAS), 2020.
- Best Paper Selection Committee Member, IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), 2020.
- TPC Member, IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2019.
- TPC Member, IEEE Nordic Circuits and Systems Conference (NORCAS), 2019.
- Best Paper Award Committee Member, IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), 2019.
- Area Co-Chair, IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), 2019.
- TC Member, Sub-TC on Smart Agriculture of the IEEE Industrial Electronics Society (IES) TC on Cloud and Wireless Systems for Industrial Applications. (2019 ~ Present)
- TPC Member, IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2018.
- Technical Track Co-Chair, IEEE International Midwest Symposium on Circuits and Systems Conference (MWSCAS) ("Analog and Mixed Signal Integrated Circuits" track, 2018).
- PC Member, 1st New Generation of Circuits and Systems Conference (NGCAS), 2017. (Sponsored by IEEE)
- PC Member, IEEE International NEW Circuits and Systems Conference (NEWCAS), 2015.
- TPC Member, International Conference on Information, Communications and Signal Processing (ICICS), 2015. (Sponsored by IEEE)
- Track Co-Chair, 22nd IFIP/IEEE International Conference on Very Large Scale Integration VLSI-SoC 2014 ("Embedded Systems and Processors, Hardware/Software Codesign" track, 2014).
- TPC Member, International Conference on Green Circuits and Systems (ICGCS), 2010. (Sponsored by IEEE)
- PC Member, International Conference on Multimedia and Ubiquitous Engineering (MUE), 2008.
- TPC Member, VLSI Design/CAD Symposium. (2008~2012)
- TPC Member, National Computer Symposium, 2007.

5) Special Session Organizer/Co-Organizer

- IEEE International System-on-Chip Conference (SOCC), 2019.
  Session Title: SOC Architecture and Circuit for IoT Applications (with Prof. Terng-Yin Hsu)
- IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2018.
  Session Title: Artificial Intelligent (AI) System and Advanced Processing (AP) Core Technology (with Prof. Hongbin Sun)
- IEEE International Conference on Digital Signal Processing (DSP), 2015.
  Session Title: Advanced Techniques and Architecture for GPU Systems

- International Conference on Information, Communications and Signal Processing (ICICS), 2013. (Sponsored by IEEE)
  Session Title: Advanced Biomedical Signal Processing Systems and 3D Multimedia System
- International Conference on Green Circuits and Systems (ICGCS), 2010.
  Session Title: Green Technologies for Reliable Circuits and Advanced Systems
- IEEE International Conference on Circuits and Systems (ISCAS), 2009.
  Session Title: Design Methodologies for Reliable Nanoscale Devices/Circuits and Advanced Gigascale/SOC Systems (with Prof. Ching-Te Chiu)

6) Session Chair/Co-Chair

- IEEE International Conference on Circuits and Systems (ISCAS). (2008~2012, 2014~2020)
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS). (2019)
- IEEE International System-on-Chip Conference (SOCC). (2019)
- IEEE Asia Pacific Conference on Circuits and Systems (APCCAS). (2018)
- IEEE International Conference on Digital Signal Processing (DSP). (2015)
- International Conference on Information, Communications and Signal Processing (ICICS). (2013)
- International Conference on Green Circuits and Systems (ICGCS). (2010)
- National Computer Symposium. (2007)
- IEEE International Conference on Systems, Man, and Cybernetics (SMC). (2006)
- VLSI Design/CAD Symposium. (2005~2006, 2008, 2010~2014)

7) Reviewer of International Journal (Over 100 Journal Papers without counting the revised submissions)

- IEEE Access. (2015, 2017)
- IEEE Embedded Systems Letters. (2013)
- IEEE Internet of Things Magazine. (2020)
- IEEE Signal Processing Letters. (2003, 2006, 2007)
- IEEE Signal Processing Magazine. (2016)
- IEEE Transactions on Biomedical Circuits and Systems. (2015)
- IEEE Transactions on Circuits and Systems I: Regular Papers. (2002, 2004, 2005, 2007~2012)
- IEEE Transactions on Circuits and Systems II: Express Briefs. (2002, 2004, 2006~2013, 2017, 2018)
- IEEE Transactions on Circuits and Systems for Video Technology. (2007, 2019)
- IEEE Transactions on Computers. (2006, 2007, 2010, 2011, 2014)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. (2011, 2017)
- IEEE Transactions on Multimedia. (2002, 2003, 2007, 2008, 2012)
- IEEE Transactions on Multi-Scale Computing Systems. (2016)
- IEEE Transactions on Neural Networks and Learning Systems. (2018)
- IEEE Transactions on Parallel and Distributed Systems. (2013)
- IEEE Transactions on Signal Processing. (2006, 2007)
- IEEE Transactions on Sustainable Computing. (2017)
- IEEE Transactions on VLSI Systems. (2004~2009, 2011, 2013~2015, 2017, 2022)
- IEEE Wireless Communications Magazine. (2017).
- ACM Transactions on Design Automation of Electronic Systems. (2011)
- Asian Journal of Control. (2008)
- ASP - Journal of Medical Imaging and Health Informatics. (2014)
- Elsevier - Computer and Electrical Engineering. (2009)
- Elsevier - Integration, The VLSI Journal. (2004, 2012, 2013, 2015, 2017)
- Elsevier - Microelectronics Journal. (2003, 2013)
- EURASIP Journal on Applied Signal Processing. (2003)
- IEE Proceedings - Computers and Digital Techniques. (2006)
- International Journal of Electrical Engineering (IJEE). (2008, 2011)

- Journal of Information Science and Engineering (JISE). (2007, 2010, 2017, 2018)
- Journal of the Chinese Institute of Engineers. (2013)
- Springer - Circuits, Systems, and Signal Processing. (2016, 2017)
- Springer - Journal of Signal Processing Systems. (2010, 2013, 2015, 2019, 2020)
- Wiley - International Journal of Circuit Theory and Applications. (2008)

8) Reviewer of International Conferences

- IEEE Asia Pacific Conference on Circuits and Systems (APCCAS).
- IEEE Biomedical Circuits and Systems Conference (BIOCAS).
- IEEE Global Communications Conference (GLOBECOM) - Symposium on Selected Areas in Communications.
- IEEE International Conference on Communications (ICC) - Signal Processing for Communications Symposium.
- IEEE International Conference on Electronics, Circuits, and Systems (ICECS).
- IEEE International Conference on Multimedia and Expo (ICME).
- IEEE International Midwest Symposium on Circuits and Systems (MWSCAS).
- IEEE International Symposium on Circuits and Systems (ISCAS).
- IEEE 14th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC).
- IEEE International Symposium on High Performance Computer Architecture (HPCA).
- IEEE TENCON.
- IEEE Workshop on Signal Processing Systems (SiPS).
- IMEKO IWADC 2011 and IEEE ADC Forum.
- International Conference on Green Circuits and Systems (ICGCS).
- International Conference on Information, Communications and Signal Processing (ICICS).
- International Conference on Intelligent Transport Systems Telecommunications (ITST).
- International Symposium on Integrated Circuits (ISIC).

9) Referee of Promotion

- IEEE Senior Member Application Review Panel. (Oct. 07, 2017)
- Assistant Professor Promotion in Taiwan x1. (2016)

10) Referee of International Project

- The Research Foundation - Flanders (Fonds Wetenschappelijk Onderzoek - Vlaanderen, FWO). (2016)

11) Referee of National Project

- Ministry of Science and Technology (MOST). (2014, 2015, 2017, 2018, 2019, 2020, 2021) [https://www.most.gov.tw/]
- Ministry of Science and Technology (MOST) - Academia-Industry Technology Alliance Collaboration Project. (Umpire, Dec. 2020) [Chinese: 科技部-產學技術聯盟合作計畫(產學小聯盟): 主審委員 x3 件]
- National Science Council (NSC). (2008, 2009, 2010) [https://www.most.gov.tw/]
- Ministry of Education (MOE) (2013, 2016). [http://www.edu.tw/]
- Ministry of Economic Affairs (MOEA). (2007, 2015, 2019) [http://www.moea.gov.tw/MNS/populace/home/Home.aspx]

12) Referee of National Contest

- TSRI Little Programmer Contest. (Jan. 2021) [Chinese: 臺灣半導體研究中心-2021 SenCu-小小程式設計師創意應用競賽: 初賽評審委員]
- NTHU-CS Undergraduate Project Demo Final Contest. (Dec. 12, 2014) [Chinese: 國立清華大學資訊工程學系大學部專題展: 決賽評審委員]
- MOE - Intelligent Electronics Design Contest. (2014 (初賽), May 10, 2014 (決賽)) [Chinese: 智慧電子系統設計競賽]
- Intel Taiwan Intelligent Systems Design Student Contest. (Oct. 2012)
- TICD Thesis Award. (2008)

- National Silicon IP Contest. (2003~2007)
- ARM Code-O-RAMA Design Contest. (2007, 2009, Apr. 2014 (初賽), May 16, 2014 (決賽))
- CIC Chip Design Award. (2007, 2010)
- MXIC Golden Silicon Awards. (2006)
- SoC Design Contest. (2004)

13) Consultant

- Technology Licensing Office, National Chiao Tung University. (2014) [Chinese:技術顧問]
- National Chip Implementation Center (CIC). (2006/02/01~2006/12/31)

14) Demo Invitation

- Make Faire Taipei, Taipei, Taiwan, May 2016.
- Intel Asia Innovation Summit, Taipei, Taiwan, 2015.
- Intel Asia Innovation Summit, Taipei, Taiwan, 2014.

15) Examiner/Referee of Dissertation/Thesis

- Chang Gung University, Taiwan (Ph. D. Dissertation).
- Chung Yuan Christian University (Ph. D. Dissertation).
- Nanyang Technological University (Ph. D. Dissertation).
- National Cheng Kung University, Taiwan (Ph. D. Dissertation, Master Thesis).
- National Chiao Tung University, Taiwan (Ph. D. Dissertation, Master Thesis).
- National Taiwan University (Ph. D. Dissertation, Master Thesis).
- National Taiwan Normal University (Master Thesis).
- National Tsing Hua University, Taiwan (Ph. D. Dissertation, Master Thesis).
- University Tunku Abdul Rahman, Malaysia (Master Thesis).
- University of Sydney (Ph. D. Dissertation).
- Tatung University, Taiwan (Ph. D. Dissertation, Master Thesis).

16) Invited Talk

- "Efficient FastICA Hardware Architectures for EEG Signal Separation", International Forum of Neuroimaging and Neuroeducation, Taiwan, Oct. 21, 2021.
- "Intelligent Swimming Detection and Tracking", AI Model for Video Prediction of AI Application Technology Online Sharing Workshop, Taiwan, Jul. 27, 2021. [Chinese: AI 應用技術線上分享會，主辦單位: 人工智慧普適研究中心、台灣雲協 AI SIG、台灣雲協技術專家委員會]
- "Efficient FastICA Algorithms and Architectures for EEG Signal Separation", at Research Center for Information Technology Innovation, Academia Sinica, Taiwan, Aug. 26, 2020.
- "Efficient FastICA Algorithms and Architectures for EEG Signal Separation", Nanyang Technological University (NTU), Singapore, Sep. 03, 2019. [Jointly organized by IEEE Circuits and Systems Singapore Chapter & IEEE Signal Processing Singapore Chapter & Centre for Infocomm Technology (INFINITUS), School of EEE, NTU]
- "AI thinks, therefore AI is: AI Overview", at NTT Data Taiwan Corporation, Ltd, Jan. 24, 2019.
- "AI thinks, therefore AI is: AI Overview", at CTCI Corporation, Dec. 26, 2018.
- "Introduction to GPU Architecture Development History", at Taichung Municipal Taichung First Senior High School, Taiwan, Apr. 11, 2018.
- "Graphics Hardware Architecture" 三維多媒體種子教師研習營暨教學研討會, at Institute of EE, National Taiwan University, Taiwan, Jan. 20, 2016.
- "Energy-Efficient FastICA Architecture and Implementation for EEG Signal Processing", at Integrated Circuits and Systems Group, National Central University, Taiwan, Jan. 07, 2015.
- "Efficient Geometry Engine Design and Case Study Implementation", 3D 多媒體課程教學研討會暨種子教師培訓營, at Institute of EE, National Taiwan University, Taiwan, Dec. 06, 2014.
- "Energy-Efficient ICA Architecture and Implementation for Biomedical Signal Processing", at Graduate Institute of Computer Science and Information Engineering, Chang Gung University, Taiwan, Jan. 08, 2014.

- "Power-Area Efficient Geometry Subsystem Design" 3D 多媒體課程教學研討會, at Institute of EE, National Taiwan University, Taiwan, Nov. 30, 2013.
- "Power-Area Efficient Geometry Subsystem Design" 3D 多媒體技術暨課程研討會, at Institute of EE, National Taiwan University, Taiwan, Nov. 18, 2012.
- "Energy-Efficient VLSI Architecture for Eight-Channel FastICA Implementation", at Swartz Center for Computational Neuroscience, UCSD, USA, Aug. 15, 2012.
- "3D Graphics System Design and Implementation" at Institute of Communications Engineering, National Tsing Hua University, Taiwan, Apr. 2010.
- "Low Power Data Format Converter Design Using Static Register Allocation", at Dept. of Electronics Engineering, National Chiao Tung University, Taiwan, Nov. 2007.
- "VLSI Architecture Design Spectrum and Case Study", at Dept. of Computer Science, National Chiao Tung University, Taiwan, Sep. 2006.
- "Recursive DFT/IDFT Design for OFDM-based Communication Systems: Algorithm and Architecture", at Dept. of Computer Science, National Chiao Tung University, Taiwan, Nov. 2005.
- "Modern VLSI Signal Processing Kernels via CIC Design Flow", at National Kaohsiung First University of Science and Technology, Taiwan, Dec. 2004.
- "Efficient VLSI Architectures for Digital Signal Processing Systems", at National Chung Cheng University, Taiwan, June, 2002.

Teaching

1) 3D Biomedical Graphics Electronic System Application Projects. (Co-teach with other professors) (Fall: 2012, 2013)
2) Digital Circuit Design. (Spring: 2017, 2018, 2019, 2021; Fall: 2007, 2009, 2010, 2011, 2012, 2017, 2018; Summer: 2019)
3) Digital Circuit Laboratory. (Fall: 2014, 2019, 2020, 2021)
4) Digital System Design. (Spring: 2009, 2011, 2012, 2014, 2015, 2016, 2017)
5) Graphics Processing Architecture and System Design. (Spring: 2013; Fall: 2011, 2014, 2016, 2018, 2021)
6) Introduction to VLSI and SOC Design. (Spring: 2008; Fall: 2008, 2009, 2013)
7) IoT Plant Care Implementation. (Microcourse, Summer 2018)
8) VLSI Digital Signal Processing. (Spring: 2006, 2007, 2010, 2020; Fall: 2008, 2010, 2015, 2017)
9) VLSI Design. (Fall: 2007)

Ph. D. Supervised

1) Tsung-Han Wu (2020/05, Co-Advisor: Prof. Yi-Bing Lin)

Dissertation Title: ElevatorTalk: A Smart Elevator Platform and Its Extension to other Applications.

2) Tsung-Che Lu (2019/06)

Dissertation Title: An Efficient Learning Computation Architecture and Implementation for Biomedical System Application.

3) Pei-Yu Chen (2018/06, Co-Advisor: Prof. Hari. C. Reddy)

Dissertation Title: Power-Efficient and Cost-Effective 2-D Symmetry Filter Architectures.

4) Di-You Wu (2012/10)

Dissertation Title: Design and Implementation of Energy-Efficient Signal Separation Systems.

Research and Teaching Project

1) [I] Yungtay - AI Intelligent Detection and Recognition System Research for Elevator Images. (PI, 1,200,000NTD, 2020/11/01 ~ 2021/04/30) [Chinese: 永大機電工業股份有限公司-電梯影像AI智能偵測辨識系統研究]
2) [G] MOST - Real-time Swimmer's Safety Monitoring and Style Identification Design by Fusing UAV Video and Wearable Data in a Mobile Device (3/3). (PI, 963,000NTD, 2022/08 ~ 2023/07) [Chinese: 科技部-於行動式裝置融合無人機視訊及穿戴式感測資訊應用於即時游泳者安全

監控及泳姿辨識設計(3/3)]

3) [G] MOST - Real-time Swimmer's Safety Monitoring and Style Identification Design by Fusing UAV Video and Wearable Data in a Mobile Device (2/3). (PI, 963,000NTD, 2021/08 ~ 2022/07) [Chinese: 科技部-於行動式裝置融合無人機視訊及穿戴式感測資訊應用於即時游泳者安全監控及泳姿辨識設計(2/3)]
4) [G] MOST - Real-time Swimmer's Safety Monitoring and Style Identification Design by Fusing UAV Video and Wearable Data in a Mobile Device (1/3). (PI, 1,010,000NTD, 2020/08 ~ 2021/07) [Chinese: 科技部-於行動式裝置融合無人機視訊及穿戴式感測資訊應用於即時游泳者安全監控及泳姿辨識設計(1/3)]
5) [G] NCTU - Hardware-Oriented Real-Time Artifact Subspace Reconstruction (ASR) Algorithm and Architecture Design for Brain-Computer Interface. (PI, 583,330NTD, 2020/01 ~ 2020/12) [Chinese: 國立交通大學-應用於腦機介面之硬體導向人工子空間重構(ASR)即時演算法及架構設計]
6) [G] MOST - Core Technologies and Application Developments for M2M Communication Systems (3/3). (PI, 8,000,000NTD, 2019/10 ~ 2020/09) [Chinese: 科技部-基於M2M聯網之核心技術與應用開發(3/3)]
7) [G] MOST - Core Technologies and Application Developments for M2M Communication Systems (2/3). (PI, 9,000,000NTD, 2018/10 ~ 2019/09) [Chinese: 科技部-基於M2M聯網之核心技術與應用開發(2/3)]
8) [G] MOST - Core Technologies and Application Developments for M2M Communication Systems (1/3). (PI, 9,000,000NTD, 2017/10 ~ 2018/09, PI from 2018/03 to 2018/09, Co-PI from 2017/10 to 2018/03) [Chinese: 科技部-基於M2M聯網之核心技術與應用開發(1/3)]
9) [G] MOST - Adjustable Low-Power 3D Rendering Hardware Architecture and System Design in Cloud Side (3/3). (PI, 860,000NTD, 2019/08 ~ 2020/07) [Chinese: 科技部-支援未來AR/VR應用的高效能繪圖系統技術-子計畫三:可調式低功耗雲端三維繪圖渲染器架構與系統設計(3/3)]
10) [G] MOST - Adjustable Low-Power 3D Rendering Hardware Architecture and System Design in Cloud Side (2/3). (PI, 877,000NTD, 2018/08 ~ 2019/07) [Chinese: 科技部-支援未來AR/VR應用的高效能繪圖系統技術-子計畫三:可調式低功耗雲端三維繪圖渲染器架構與系統設計(2/3)]
11) [G] MOST - Adjustable Low-Power 3D Rendering Hardware Architecture and System Design in Cloud Side (1/3). (PI, 895,000NTD, 2017/08 ~ 2018/07) [Chinese: 科技部-支援未來AR/VR應用的高效能繪圖系統技術-子計畫三:可調式低功耗雲端三維繪圖渲染器架構與系統設計(1/3)]
12) [I] CTCI - Intelligent Technology Development Research with Applications to the Construction Site Management - Drone Technology Development for Construction-Site Autonomous Navigation and Helmet Wearing Detection. (PI, 1,200,000NTD, 2019/07/01 ~ 2019/12/31) [Chinese: 中鼎工程股份有限公司-智能科技協助建造場域管理之開發研究-無人機工地自動巡航與安全帽配戴偵測技術開發]
13) [I] CTCI - Intelligent Technology Development Research with Applications to the Construction Site Management – Use Drone with BIM to Track the Construction Schedule. (PI, 800,000NTD, 2019/08/01 ~ 2020/01/31) [Chinese: 中鼎工程股份有限公司-智能科技協助建造場域管理之開發研究-運用空拍機與BIM以輔助工程進度追蹤]
14) [I] CTCI - Intelligent Technology Development Research with Applications to the Construction Site Management - IoT Applications to the Construction Site Storage. (PI, 600,000NTD, 2019/06/01 ~ 2019/12/31) [Chinese: 中鼎工程股份有限公司-智能科技協助建造場域管理之開發研究-工地倉儲IoT應用]
15) [I] CTCI - Intelligent Device Development Research with Applications to the Construction Site Management - Drone Technology Development with Applications to the Construction Site. (PI,

1,200,000NTD, 2018/01/01 ~ 2018/12/31) [Chinese: 中鼎工程股份有限公司-智能化裝置於建造工地管理之開發研究 for 無人機於工地之應用技術開發]

16) [I] CTCI - Intelligent Device Development Research with Applications to the Construction Site Management - IoT Technology Development with Applications to the Construction Site Storage: Allocations of Wooden Box, Cable Drum, Pallet. (PI, 1,000,000NTD, 2018/01/01 ~ 2018/12/31) [Chinese: 中鼎工程股份有限公司-智能化裝置於建造工地管理之開發研究-工地倉儲IoT應用技術開發-木箱、Cable Drum、棧板定位]
17) [G] NCTU - Silicon Valley Top Laboratory Student Internship Program. (PI, 530,000NTD, 2018/01 ~ 2018/12) [Chinese: 國立交通大學-矽谷頂尖實驗室學生實習計畫]
18) [F] ITRI - Breathing Feature Extraction and Estimation of COPD Monitoring System. (PI, 600,000NTD, 2017/10/01 ~ 2018/3/31)
19) [I] CTCI - Intelligent Sensing Technology Research with Applications to the Construction Site Management. (PI, 2,800,000NTD, 2017/01/01 ~ 2017/12/31) [Chinese: 中鼎工程股份有限公司-智慧感測科技應用於工地管理之研究]
20) [F] NARL-CIC - iOS based APP Research for the MorSensor IR Ranger and Color Sensing System. (PI, 160,000NTD, 2017/08/01 ~ 2017/11/30)
21) [F] NARL-CIC - iOS based APP Research for the MorSensor Ultrasonic Ranger. (PI, 80,000NTD, 2017/04/10 ~ 2017/07/10)
22) [G] MOST - A Reconfigurable 3D Graphics Processor Design for Hybrid Rendering of Ray-Tracing and Rasterization (3/3). (PI, 770,000NTD, 2016/08 ~ 2017/07) [Chinese: 科技部-支援光線追蹤圖形應用之異質多核心終端軟硬體平臺-子計畫二:支援混合光線追蹤與光柵式渲染繪圖顯示之可重組三維繪圖處理器設計(3/3)]
23) [G] MOST - A Reconfigurable 3D Graphics Processor Design for Hybrid Rendering of Ray-Tracing and Rasterization (2/3). (PI, 770,000NTD, 2015/08 ~ 2016/07) [Chinese: 科技部-支援光線追蹤圖形應用之異質多核心終端軟硬體平臺-子計畫二:支援混合光線追蹤與光柵式渲染繪圖顯示之可重組三維繪圖處理器設計(2/3)]
24) [G] MOST - A Reconfigurable 3D Graphics Processor Design for Hybrid Rendering of Ray-Tracing and Rasterization (1/3). (PI, 770,000NTD, 2014/08 ~ 2015/07) [Chinese: 科技部-支援光線追蹤圖形應用之異質多核心終端軟硬體平臺-子計畫二:支援混合光線追蹤與光柵式渲染繪圖顯示之可重組三維繪圖處理器設計(1/3)]
25) [G] NSC - A Programmable 3D Graphics Processor Design for Client-Side Multi-Core Embedded Systems (3/3). (PI, 1,081,000NTD, 2013/05 ~ 2014/07) [Chinese: 國家科學委員會-以圖型應用為主的用戶端多核心嵌入式系統-子計畫四：用戶端多核心嵌入式系統可程式化三維圖型處理器設計(3/3)]
26) [G] NSC - A Programmable 3D Graphics Processor Design for Client-Side Multi-Core Embedded Systems (2/3). (PI, 991,000NTD, 2012/05 ~ 2013/04) [Chinese: 國家科學委員會-以圖型應用為主的用戶端多核心嵌入式系統-子計畫四：用戶端多核心嵌入式系統可程式化三維圖型處理器設計(2/3)]
27) [G] NSC - A Programmable 3D Graphics Processor Design for Client-Side Multi-Core Embedded Systems (1/3). (PI, 926,000NTD, 2011/05 ~ 2012/04) [Chinese: 國家科學委員會-以圖型應用為主的用戶端多核心嵌入式系統-子計畫四：用戶端多核心嵌入式系統可程式化三維圖型處理器設計(1/3)]
28) [G] NSC - Design Integration of Biomedical Signal Processor and Multiple Biomedical Information Display based on Next-Generation Intelligent ICU (3/3). (PI, 826,000NTD, 2013/05 ~ 2014/07) [Chinese: 國家科學委員會-次世代智慧型加護病房照護系統-子計畫八：基於次世代智慧型ICU之生醫訊號處理器與多重生醫資訊顯示整合設計(3/3)]
29) [G] NSC - Design Integration of Biomedical Signal Processor and Multiple Biomedical Information Display based on Next-Generation Intelligent ICU (2/3). (PI, 673,000NTD, 2012/05 ~ 2013/04) [Chinese: 國家科學委員會-次世代智慧型加護病房照護系統-子計畫八：基於次世

代智慧型ICU之生醫訊號處理器與多重生醫資訊顯示整合設計(2/3)]

30) [G] NSC - Design Integration of Biomedical Signal Processor and Multiple Biomedical Information Display based on Next-Generation Intelligent ICU (1/3). (PI, 752,000NTD, 2011/05 ~ 2012/04) [Chinese: 國家科學委員會-次世代智慧型加護病房照護系統-子計畫八：基於次世代智慧型ICU之生醫訊號處理器與多重生醫資訊顯示整合設計(1/3)]
31) [G] NCTU Project of Research Competency Enhancement for Young Professor - Power-efficient On-line Multi-mode Hilbert-Huang Transform Hardware Design and Implementation for Biomedical Signals. (PI, 2012/04 ~ 2012/12)
32) [G] NCTU - Top 100 University Collaboration Project - Real-Time Non-Switch FastICA Design and Implementation. (PI, 200,000NTD, 2012/04 ~ 2012/12) [Chinese: 國立交通大學-國際百大合作計畫: 即時高穩定性8通道FastICA設計與實現]
33) [I] ASUS - Application Services in Heterogeneous Cloud Platform. (PI, 1,740,000NTD, 2010/09 ~ 2011/08) [Chinese: 華碩電腦股份有限公司-異質雲端平台之應用服務]
34) [G] NSC - Low-Complexity Biomedical Computation Engine Design and Embedded Platform Development (3/3). (PI, 882,000NTD, 2010/08 ~ 2011/07) [Chinese: 國家科學委員會-可攜式EEG/EKG/fNIRS腦神經影像系統研發暨其整合型生醫感測處理晶片系統設計-子計畫四：低複雜度生醫運算引擎設計與嵌入式平台建置(3/3)]
35) [G] NSC - Low-Complexity Biomedical Computation Engine Design and Embedded Platform Development (2/3). (PI, 882,000NTD, 2009/08 ~ 2010/07) [Chinese: 國家科學委員會-可攜式EEG/EKG/fNIRS腦神經影像系統研發暨其整合型生醫感測處理晶片系統設計-子計畫四：低複雜度生醫運算引擎設計與嵌入式平台建置(2/3)]
36) [G] NSC - Low-Complexity Biomedical Computation Engine Design and Embedded Platform Development (1/3). (PI, 882,000NTD, 2008/08 ~ 2009/07) [Chinese: 國家科學委員會-可攜式EEG/EKG/fNIRS腦神經影像系統研發暨其整合型生醫感測處理晶片系統設計-子計畫四：低複雜度生醫運算引擎設計與嵌入式平台建置(1/3)]
37) [G] NSC - Smart Sensor SoC Design and Embedded Wireless Biomedical Platform Development (I). (PI, 503,000NTD, 2007/08 ~ 2008/07) [Chinese: 國家科學委員會-結合生物反饋之新世代腦機介面及其在移動載具控制之應用-子計畫二：智慧型感測系統單晶片設計與嵌入式無線生醫平台開發(I)]
38) [G] MOST - Pervasive AI Services: Developing Intelligent Agents to Drive Digital Transformations (1/2). (Co-PI, 23,000,000NTD, 2021/11 ~ 2022/10) [Chinese: 科技部-普適AI服務：數位轉型趨勢下的智慧型代理人(1/2)]
39) [G] MOST - On Self-Maneuvered Patrolling Robots with Artificial Intelligence and Multi-Sensory Data Fusion Technology (4/4). (Co-PI, 10,750,000NTD, 2021/01 ~ 2021/12) [Chinese: 科技部-基於人工智能融合技術集成多元環境感測的導引及巡邏機器人(4/4)]
40) [G] MOST - On Self-Maneuvered Patrolling Robots with Artificial Intelligence and Multi-Sensory Data Fusion Technology (3/4). (Co-PI, 10,930,000NTD, 2020/01 ~ 2020/12) [Chinese: 科技部-基於人工智能融合技術集成多元環境感測的導引及巡邏機器人(3/4)]
41) [G] MOST - On Self-Maneuvered Patrolling Robots with Artificial Intelligence and Multi-Sensory Data Fusion Technology (2/4). (Co-PI, 10,920,000NTD, 2019/01 ~ 2019/12) [Chinese: 科技部-基於人工智能融合技術集成多元環境感測的導引及巡邏機器人(2/4)]
42) [G] MOST - On Self-Maneuvered Patrolling Robots with Artificial Intelligence and Multi-Sensory Data Fusion Technology (1/4). (Co-PI, 10,200,000NTD, 2018/01 ~ 2018/12) [Chinese: 科技部-基於人工智能融合技術集成多元環境感測的導引及巡邏機器人(1/4)]
43) [G] NCSIST – Automatically Recognizing and Tracking Technologies for Smart Drone (1/3). (Co-PI, 2019/05 ~ 2019/11) [Chinese: 國家中山科學研究院-智慧化無人機群自動辨識及追蹤技術(1/3)]
44) [G] MOST - Field Trial with Koala Wearable Device Applications. (Co-PI, 3,176,000NTD, 2017/08 ~ 2018/07) [Chinese: 科技部-Koala穿戴裝置雲端服務場域驗證-Koala穿戴裝置雲端

服務場域驗證]

45) [G] MOST - Design and Development of IoT and Wearable system for Health Monitoring of Seniors. (Co-PI, 543,000NTD, 2017/08 ~ 2018/07) [Chinese: 科技部-發展物聯網以及穿戴式系統應用於銀髮族之健康監控以及照護]
46) [G] MOST - Adaptive Server-Client Runtime for Future VR/AR Applications (3/3). (Co-PI, 1,458,000NTD, 2019/08 ~ 2020/07) [Chinese: 科技部-支援未來AR/VR應用的高效能繪圖系統技術-總計畫暨子計畫一:支援虛擬擴增實境之可適性雲端終端執行期軟體程式庫(3/3)]
47) [G] MOST - Adaptive Server-Client Runtime for Future VR/AR Applications (2/3). (Co-PI, 1,435,000NTD, 2018/08 ~ 2019/07) [Chinese: 科技部-支援未來AR/VR應用的高效能繪圖系統技術-總計畫暨子計畫一:支援虛擬擴增實境之可適性雲端終端執行期軟體程式庫(2/3)]
48) [G] MOST - Adaptive Server-Client Runtime for Future VR/AR Applications (1/3). (Co-PI, 1,433,000NTD, 2017/08 ~ 2018/07) [Chinese: 科技部-支援未來AR/VR應用的高效能繪圖系統技術-總計畫暨子計畫一:支援虛擬擴增實境之可適性雲端終端執行期軟體程式庫(1/3)]
49) [G] MOST - Core Technologies and Application Developments for M2M Communication Systems. (Co-PI, 10,000,000NTD, 2016/10 ~ 2017/09) [Chinese: 科技部-基於M2M聯網之核心技術與應用開發]
50) [G] MOST - Memory and Multicore System Architecture of Processing in Memory with Non-Volatility (3/3). (Co-PI, 1,184,000NTD, 2016/08 ~ 2017/07) [Chinese: 科技部-結合非揮發性之多核心系統與記憶體架構(3/3)]
51) [G] MOST - Memory and Multicore System Architecture of Processing in Memory with Non-Volatility (2/3). (Co-PI, 892,000NTD, 2015/08 ~ 2016/07) [Chinese: 科技部-結合非揮發性之多核心系統與記憶體架構(2/3)]
52) [G] MOST - Memory and Multicore System Architecture of Processing in Memory with Non-Volatility (1/3). (Co-PI, 869,000NTD, 2014/08 ~ 2015/07) [Chinese: 科技部-結合非揮發性之多核心系統與記憶體架構(1/3)]
53) [G] MOST - Cloud and Big Data Computing Platforms for M2M Communications Systems. (Co-PI, 9,000,000NTD, 2015/01 ~2015/12) [Chinese: 科技部-基於M2M聯網之雲端與巨量資料運算平台開發(2/3)]
54) [G] MOST - Cloud and Big Data Computing Platforms for M2M Communications Systems. (Co-PI, 9,000,000NTD, 2014/01 ~2014/12) [Chinese: 科技部-基於M2M聯網之雲端與巨量資料運算平台開發(1/3)]
55) [G] MOE - Intelligent Electronics Talent Cultivation Program - Application Processors Education Consortium. (Co-PI (執行秘書), 3,359,507NTD, 2015/03/01 ~ 2016/04/30) [Chinese: 教育部-智慧電子整合性人才培育計畫-高階應用處理器(AP)聯盟中心計畫]
56) [G] MOE - Intelligent Electronics Talent Cultivation Program - Application Processors Education Consortium. (Co-PI (執行秘書), 3,154,549NTD, 2014/03/01 ~ 2015/02/28) [Chinese: 教育部-智慧電子整合性人才培育計畫-高階應用處理器(AP)聯盟中心計畫]
57) [G] MOE - Intelligent Electronics Talent Cultivation Program - Application Processors Education Consortium. (Co-PI (執行秘書), 3,292,000NTD, 2012/12/01 ~ 2014/02/28) [Chinese: 教育部-智慧電子整合性人才培育計畫-高階應用處理器(AP)聯盟中心計畫]
58) [G] MOE - Intelligent Electronics Talent Cultivation Program - 4C Electronics Education Consortium. (Co-PI (執行秘書), 2,495,065NTD, 2012/04/01 ~ 2013/02/28, Co-PI from 2012/07 to 2013/02) [Chinese: 教育部-智慧電子整合性人才培育計畫-4C電子聯盟中心計畫]
59) [G] NSC - System Software and System Simulation for Client Side Multicore Based Embedded Systems (3/3). (Co-PI, 2,228,000NTD, 2013/05 ~ 2014/07) [Chinese: 國家科學委員會-以圖形應用為主的用戶端多核心嵌入式系統-總計畫及子計畫三：用戶端多核心嵌入式系統程式發展工具與系統模擬(3/3)]
60) [G] NSC - System Software and System Simulation for Client Side Multicore Based Embedded

Systems (2/3). (Co-PI, 2,441,000NTD, 2012/05 ~ 2013/04) [Chinese: 國家科學委員會-以圖形應用為主的用戶端多核心嵌入式系統-總計畫及子計畫三：用戶端多核心嵌入式系統程式發展工具與系統模擬(2/3)]

61) [G] NSC - System Software and System Simulation for Client Side Multicore Based Embedded Systems (1/3). (Co-PI, 1,601,000NTD, 2011/05 ~ 2012/04) [Chinese: 國家科學委員會-以圖型應用為主的用戶端多核心嵌入式系統-總計畫：以圖型應用為主的用戶端多核心嵌入式系統(1/3)]
62) [G] NSC - Medical Research and Development of Temporal-, Frequency- and Spatial-Domain Modality by Using HHT/PRLS Based on Cloudlet Server on Chip (3/3). (Co-PI, 1,227,000NTD, 2013/05 ~ 2014/07) [Chinese: 國家科學委員會-GreenArmy：綠色微雲伺服系統晶片平台技術-子計畫七：基於綠色微雲伺服系統晶片之HHT/PRLS 分析法實現醫用時域、頻域與空間域解析技術(3/3)]
63) [G] NSC - Medical Research and Development of Temporal-, Frequency- and Spatial-Domain Modality by Using HHT/PRLS Based on Cloudlet Server on Chip (2/3). (Co-PI, 1,202,000NTD, 2012/05 ~ 2013/04) [Chinese: 國家科學委員會-GreenArmy：綠色微雲伺服系統晶片平台技術-子計畫七：基於綠色微雲伺服系統晶片之HHT/PRLS 分析法實現醫用時域、頻域與空間域解析技術(2/3)]
64) [G] NSC - Medical Research and Development of Temporal-, Frequency- and Spatial-Domain Modality by Using HHT/PRLS Based on Cloudlet Server on Chip (1/3). (Co-PI, 1,184,000NTD, 2011/05 ~ 2012/04) [Chinese: 國家科學委員會-GreenArmy：綠色微雲伺服系統晶片平台技術-子計畫七：基於綠色微雲伺服系統晶片之HHT/PRLS 分析法實現醫用時域、頻域與空間域解析技術(1/3)]
65) [G] NSC - Detection of Hardware Trojan. (Co-PI, 860,000NTD, 2012/01 ~ 2012/12) [Chinese: 國家科學委員會-硬體惡意行為檢測技術研究]
66) [G] NSC - Detection of Hardware Trojan. (Co-PI, 561,000NTD, 2011/01 ~ 2011/12) [Chinese: 國家科學委員會-硬體惡意行為檢測技術研究]
67) [G] NSC - Advanced Green Energy DOT/EEG/ECG Heart-Brain System on Chip and Embedded systems for Integrated Brain-Heart Health Care Systems Key Technology. (Co-PI, 6,815,000NTD, 2010/11 ~ 2011/07) [Chinese: 國家科學委員會-具前瞻性綠能功能之DOT/EEG/EKG腦心健康照護系統晶片暨嵌入式系統關鍵技術]
68) [G] NSC - System Development and SoC Design of a Truly Portable Neuroimaging System Based on EEG/EKG/fNIRS Multisensors (3/3). (Co-PI, 1,254,000NTD, 2010/08 ~ 2011/07)
69) [G] NSC - System Development and SoC Design of a Truly Portable Neuroimaging System Based on EEG/EKG/fNIRS Multisensors (2/3). (Co-PI, 1,254,000NTD, 2009/08 ~ 2010/07)
70) [G] NSC - System Development and SoC Design of a Truly Portable Neuroimaging System Based on EEG/EKG/fNIRS Multisensors (1/3). (Co-PI, 1,154,000NTD, 2008/08 ~ 2009/07)
71) [G] NSC - Design of a DVB-MHP Platform with an Extension for 3-D Video Support (3/3). (Co-PI, 4,231,000NTD, 2009/11 ~ 2010/10) [Chinese: 國家科學委員會-支援3-D立體視訊的數位電視多媒體平台設計(3/3)]
72) [G] NSC - Design of a DVB-MHP Platform with an Extension for 3-D Video Support (2/3). (Co-PI, 4,417,000NTD, 2008/11 ~ 2009/10) [Chinese: 國家科學委員會-支援3-D立體視訊的數位電視多媒體平台設計(2/3)]
73) [G] NSC - Design of a DVB-MHP Platform with an Extension for 3-D Video Support (1/3). (Co-PI, 4,387,000NTD, 2007/11 ~ 2008/10) [Chinese: 國家科學委員會-支援3-D立體視訊的數位電視多媒體平台設計(1/3)]
74) [G] MOEA - Hermes - Pervasive Wireless Transceiver System Cores: Multimode MIMO-OFDM Wireless Communication System Research Development and IC Design (3/3). (Participating Professor, 14,603,000NTD, 2007/10/01 ~ 2008/09/30) [Chinese: 經濟部-信使-遍佈式無線傳收機系統核心: 多模MIMO-OFDM無線通訊系統之研發與晶片設計三年計畫(3/3)]

75) [G] MOEA - Hermes - Pervasive Wireless Transceiver System Cores: Multimode MIMO-OFDM Wireless Communication System Research Development and IC Design (2/3). (Participating Professor, 12,850,000NTD, 2006/10/01 ~ 2007/09/30) [Chinese: 經濟部-信使-遍佈式無線傳收機系統核心: 多模MIMO-OFDM無線通訊系統之研發與晶片設計三年計畫(2/3)]

Note: G: Government; I: Industry; F: Foundation; PI: Principal Investigator.

Donation

[F] Yungtay Culture and Education Public Welfare Foundation - Epidemic Prevention Elevator. (PI, 400,000NTD, 2020/06/02) [Chinese: 財團法人永大文教公益基金會-全方位+0 防疫電梯暨公益捐贈記者會]

Honor/Certificate

1) 2022 Private Chien Tai Senior High School Outstanding Alumni. [Chinese: 2022 年苗栗縣私立建臺高級中學傑出校友。(學術研究類)]
2) 2021 National Yang Ming Chiao Tung University Teachers and Researchers Globalization Research Award. [Chinese: 2021 年國立陽明交通大學教師及研究人員國際化研究成果獎勵]
3) 2021 National Yang Ming Chiao Tung University Outstanding Research Award. [Chinese: 2021 年國立陽明交通大學延攬及留住特殊優秀人才彈性薪資暨獎勵補助。(研究類, 2021/08 ~ 2023/07)]
4) Higher Education Academy (HEA) Fellow. (2021/09/03 ~ Present)
5) 2021 National Yang Ming Chiao Tung University: Mentoring Award. [Chinese: 國立陽明交通大學績優導師]
6) IEEE Access features our published article, "Green Elevator Scheduling Based on IoT Communications" as the IEEE Access "Article of the Week" on our website and social media platforms. [https://ieeeaccess.ieee.org/featured-articles/green_elevatoriot/ ; Jan. 09, 2021]
7) 2020 National Chiao Tung University Teachers and Researchers Globalization Research Award. [Chinese: 2020 年國立交通大學教師及研究人員國際化研究成果獎勵]
8) 2020 National Chiao Tung University: Mentoring Award. [Chinese: 國立交通大學績優導師]
9) 2019 National Chiao Tung University Teachers and Researchers Globalization Research Award. [Chinese: 2019 年國立交通大學教師及研究人員國際化研究成果獎勵]
10) 2018 National Chiao Tung University Teachers and Researchers Globalization Research Award. [Chinese: 2018 年國立交通大學教師及研究人員國際化研究成果獎勵]
11) 2018 MOEA - Industrial Development Bureau: Mobileheroes Communication Contest – Intelligent-of-Things Innovative Application Contest, Honorable Mention. (Co-supervisor with Dr. Yi-Bing Lin; Domestic Contest.) [Chinese: 經濟部工業局: 2018 通訊大賽-智慧聯網創新應用競賽: 佳作]
12) 2018 NCTU x acer IoT Contest, Corporate Special Award. (As a supervisor; NCTU Contest) [Chinese: 2018 NCTU x acer 物聯網競賽−企業特別獎]
13) 2017 National Chiao Tung University: Mentoring Award. [Chinese: 國立交通大學績優導師]
14) 2016 NARL - CIC - Morsensor Innovation and Application Design Contest, 2nd Place. (Co-supervisor with Dr. Yun-Wei Lin; Domestic Contest.) [Chinese: 財團法人國家實驗研究院-國家晶片系統設計中心(CIC) 2016 MorSensor 無線感測積木創意應用設計競賽: 銀牌。]
15) 2016 MOEA - Industrial Development Bureau: Mobileheroes Communication Contest – MediaTek IoT Development Contest, Honorable Mention. (Co-supervisor with Dr. Yun-Wei Lin; Domestic Contest.) [Chinese: 經濟部工業局: 2016 通訊大賽-聯發科技物聯網開發競賽: 佳作]
16) 2016 Acer-NCTU aBeing Application and Implementation Contest, 2nd Place. (As a supervisor; NCTU Contest) [Chinese: 2016 宏碁-交通大學 aBeing 應用實作競賽: 第 2 名]

17) IEEE Senior Member. (2016 ~ Present)
18) 2015 NARL - CIC - Morsensor Innovation and Application Design Contest, Honorable Mention. (As a supervisor; Domestic Contest.) [Chinese: 財團法人國家實驗研究院 - 國家晶片系統設計中心(CIC) - 2015 MorSensor 無線感測積木創意應用設計競賽:佳作]
19) 2015 MOEA - Department of Commerce: Wearable Magic Future: Demo Technology Innovation Sharing Campus Workshop Contest, 2nd Place. (Co-supervised with Prof. Y. C. Tseng; Domestic Contest.) [Chinese: 經濟部商業司:「穿戴」起不可思議的未來 - 104 年度展示科技創意分享校園工作坊競賽: 第二名]
20) 2015 NCTU-Contest of Innovative IoT/M2M Service based on Reusable Platforms, 2nd Place. (As a supervisor; The teams from other universities in Taiwan can join this domestic contest.) [Chinese: 亞軍]
21) 2015 NCTU-Contest of Innovative IoT/M2M Service based on Reusable Platforms, 3rd Place. (As a supervisor; The teams from other universities in Taiwan can join this domestic contest.) [Chinese: 季軍]
22) 2014 Intel Taiwan Intelligent Systems Design Student Contest, 1st Place. (As a supervisor; Domestic Contest.) [Chinese: 冠軍]
23) J. W. Qiu, T. H. Chiang, C. C. Lo, L. M. Lin, L. D. Van, Y. C. Tseng, and Y. T. Ching, "Continuous human location and posture tracking by multiple depth sensors," in *Proc. IEEE International Conference on Internet of Things (iThings 2014)*, Best Paper Award. [Chinese: 最佳論文獎]
24) 2014 NCTU-Contest of Innovative IoT/M2M Service based on Reusable Platforms, 1st Place. (As a supervisor; The teams from other universities in Taiwan can join this domestic contest.) [Chinese: 冠軍]
25) 2014 NCTU-Contest of Innovative IoT/M2M Service based on Reusable Platforms, 3rd Place. (As a supervisor; The teams from other universities in Taiwan can join this domestic contest.) [Chinese: 季軍 x2]
26) 2014 NCTU-Contest of Innovative IoT/M2M Service based on Reusable Platforms, Honorable Mention. (As a supervisor; The teams from other universities in Taiwan can join this domestic contest.) [Chinese: 佳作]
27) 2014 College of Computer Science, National Chiao Tung University: Teaching Award. [Chinese: 國立交通大學資訊學院教學獎]
28) 2013 MOE - Intelligent Electronics Talent Cultivation Program - 4C Electronics Contest Field, 1st Place. (Co-supervised with Prof. Y. S. Wang; Domestic Contest.) [Chinese: 特優]
29) 2012 National IC Design Contest - Standard Cell Digital Design Group for Graduate, 4th Place. (As a supervisor) [Chinese: 設計完成獎]
30) 2011 National Chiao Tung University Outstanding Research Award. [Chinese: 2011 年國立交通大學延攬及留住特殊優秀人才彈性薪資暨獎勵補助。(研究類, 2011/08 ~ 2013/07)]
31) 2010 National IC Design Contest - Standard Cell Digital Design Group for Graduate, Honorable Mention. (As a supervisor) [Chinese: 佳作]
32) 2010 National IC Design Contest - Full-Custom Design Group for Graduate, 4rd Place. (As a supervisor) [Chinese: 設計完成獎]
33) 2010 National Embedded System Design Contest - Hardware/Software Integration Group, Honorable Mention. (Co-supervised with Prof. C. J. Tsai) [Chinese: 佳作]
34) 2007 ARM Code-O-Rama Design Contest, 3rd Place. (As a supervisor; Domestic Contest) [Chinese: 季軍]
35) 2006 National Embedded Software Design Contest - Application Group, Honorable Mention. (Co-supervised with Prof. C. T. Lin) [Chinese: 佳作]
36) C. A. Tsai, Y. T. Chou, Y. T. Chang, L. D. Van, and C. M. Huang, "ARM-based SoC prototyping platform using Aptix," in *Proc. iNEER Conference for Engineering Education and Research (iCEER)*, Mar. 2005, Tainan, Taiwan, Best Poster Award.

37) 2004 National Chip Implementation Center (CIC) Outstanding Award. (Rate= 3.8%)
38) 2001 IEEE Award for outstanding leadership and service to the National Taiwan University Student Branch.
39) Motorola Scholarship. (Jan. 1997; Domestic Scholarship.)
40) Chunghwa Picture Tube Scholarship. (Oct. 1995; Domestic Scholarship.)
41) First Honor of Dept. of Electrical Engineering, Tatung Institute of Technology with 183 credits. (1995)
42) Tatung Institute of Technology Academic Achievement Scholarship. [Chinese: 書卷獎]

Publication

Journal Papers

[1] Lan-Da Van, Y. C. Tu, C. Y. Chang, H. J. Wang, and T. P. Jung "Hardware-oriented memory-limited online artifact subspace reconstruction (HMO-ASR) algorithm," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 12, pp. 3493-3497, Dec. 2021.

[2] Lan-Da Van, L. Y. Zhang, C. H. Chang, K. L. Tong, K. R. Wu, and Y. C. Tseng, "Things in the air: Tagging IoT information on drone videos," *Discover Internet of Things*, vol. 1, issue 1, Feb. 2021.

[3] Lan-Da Van, Y. B. Lin, T. H. Wu, and Y. C. Lin, "An intelligent elevator development and management system," *IEEE Systems Journal*, vol. 14, no. 2, pp. 3015-3026, Jun. 2020.

[4] Lan-Da Van, Y. B. Lin, T. H. Wu, and T. H. Chao, "Green elevator scheduling based on IoT communications," *IEEE Access*, vol. 8, pp. 38404-38415, Mar. 2020.

[5] Lan-Da Van, Y. B. Lin, T. H. Wu, Y. W. Lin, S. R. Peng, L. H. Kao, C. H. Chang, "PlantTalk: A smartphone-based intelligent hydroponic plant box," *Sensors*, vol. 19, issue 8, Apr. 2019.

[6] Lan-Da Van, I. H. Khoo, P. Y. Chen, and H. C. Reddy, "Symmetry incorporated cost-effective architectures for two-dimensional digital filters," *IEEE Circuits and Systems Magazine*, vol. 19, issue 1, pp. 33-54, Q1, 2019.

[7] C. C. Chiu, Lan-Da Van, and Y. S. Lin, "Efficient progressive radiance estimation engine architecture and implementation for progressive photon mapping," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 8, pp. 2491-2502, Aug. 2018.

[8] Lan-Da Van, P. Y. Huang, and T. C. Lu "Cost-effective and variable-channel FastICA hardware architecture and implementation for EEG signal processing," *Journal of Signal Processing Systems*, vol. 82, issue 1, pp. 91-113, Jan. 2016.

[9] I. H. Khoo, H. C. Reddy, Lan-Da Van, and C. T. Lin, "General formulation of shift and delta operator based 2-D VLSI filter structures without global broadcast and incorporation of the symmetry," *Multidimensional Systems and Signal Processing*, vol. 25, issue 4, pp. 795-828, Oct. 2014.

[10] Lan-Da Van, D. Y. Wu, and C. S. Chen, "Energy-efficient FastICA implementation for biomedical signal separation," *IEEE Transactions on Neural Networks*, vol. 22, no. 11, pp. 1809-1822, Nov. 2011.

[11] Lan-Da Van and T. Y. Sheu, "A power-area efficient geometry engine with low-complexity subdivision algorithm for 3D graphics system," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 9, pp. 2211-2224, Sep. 2011.

[12] D. Y. Wu and Lan-Da Van, "Efficient detection algorithms for MIMO communication systems," *Journal of Signal Processing Systems*, vol. 62, issue 3, pp. 427-442, Mar. 2011.

[13] P. Y. Chen, Lan-Da Van, I. H. Khoo, H. C. Reddy, and C. T. Lin, "Power-efficient and cost-effective 2-D symmetry filter architectures," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 112-125, Jan. 2011.

[14] J. H. Tu and Lan-Da Van, "Power-efficient pipelined reconfigurable fixed-width Baugh-Wooley multipliers," *IEEE Transactions on Computers*, vol. 58, no. 10, pp. 1346-1355, Oct. 2009.

[15] C. T. Lin, Y. C. Yu, and Lan-Da Van, "Cost-effective triple-mode reconfigurable pipeline FFT/IFFT/2-D DCT processor," *IEEE Transactions on VLSI Systems*, vol. 16, no. 8, pp. 1058-1071, Aug. 2008.

[16] Lan-Da Van, C. T. Lin, and Y. C. Yu, "VLSI architecture for the low-computation cycle and power-efficient recursive DFT/IDFT design," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E90-A, no. 8, pp. 1644-1652, Aug. 2007.

[17] M. A. Song, Lan-Da Van, and S. Y. Kuo, "Adaptive low-error fixed-width Booth multipliers," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E90-A, no. 6, pp. 1180-1187, Jun. 2007.

[18] Lan-Da Van and C. C. Yang, "Generalized low-error area-efficient fixed-width multipliers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no.8, pp. 1608-1619, Aug. 2005.

[19] Lan-Da Van, "A new 2-D systolic digital filter architecture without global broadcast," *IEEE Transactions on VLSI Systems*, vol. 10, no. 4, pp. 477-486, Aug. 2002.

[20] Lan-Da Van and W. S. Feng, "An efficient systolic architecture for the DLMS adaptive filter and its applications," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 4, pp. 359-366, Apr. 2001.

[21] Lan-Da Van, S. S. Wang, and W. S. Feng, "Design of the lower error fixed-width multiplier and its application," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 10, pp. 1112-1118, Oct. 2000. (Brief)

Book Edited

[1] Intel® Atom™ Platform: Intelligent Systems Development and Applications, Editor: Lan-Da Van, Library & Book, 2014. (in Traditional Chinese, Sponsored by Intel, ISBN 978-986-90988-3-0)

International Conference Papers

[1] Lan-Da Van, T. J. Wang, S. J. Tzeng, and T. P. Jung, "A computation-aware TPL utilization procedure for parallelizing the FastICA algorithm on a multi-core CPU," in *Proc. IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC)*, Dec. 2021, Singapore, accepted. (Hybrid Conference)

[2] A. B. Christian, C. Y. Lin, Lan-Da Van, and Y. C. Tseng, "Data fusion driven lane-level precision data transmission for V2X road applications," in *Proc. IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC)*, Dec. 2021, Singapore, accepted. (Hybrid Conference)

[3] T. A. Huang, S. K. Wong, and Lan-Da Van, "Trajectory-based dynamic handwriting recognition using fusion neural network," in *Proc. International Conference on Technologies and Applications of Artificial Intelligence (TAAI)*, Nov. 2021, Taichung, Taiwan, accepted.

[4] S. Sharma, A. V. V. Susmitha, Lan-Da Van, and Y. C. Tseng, "An edge-controlled outdoor autonomous UAV for colorwise safety helmet detection and counting of workers in construction sites," in *Proc. IEEE Vehicular Technology Conference (VTC-Fall)*, Sep. 2021, pp. 1-5. (Virtual Conference)

[5] A. B. Christian, C. Y. Lin, C. W. Lee, Lan-Da Van, and Y. C. Tseng, "A neural network-based multisensor data fusion approach for enabling situational awareness of vehicles," in *Proc. International Conference on Pervasive Artificial Intelligence (ICPAI)*, Dec. 2020, pp. 199-205, Taipei, Taiwan.

[6] Lan-Da Van, C. H. Chang, K. L. Tong, K. R. Wu, L. Y. Zhang, and Y. C. Tseng, "Demo: Tagging IoT data in a drone view," in *Proc. ACM Annual International Conference on Mobil Computing and Networking (MobiCom)*, Oct. 2019, pp. 1-3, Los Cabos, Mexico.

[7] Lan-Da Van, T. C. Lu, T. P. Jung, and J. F. Wang, “Hardware-oriented memory-limited online FastICA algorithm and hardware architecture for signal separation,” in *Proc. IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, May 2019, pp. 1438-1442, Brighton, UK.
[8] T. C. Lu, C. L. Lin, P. Y. Chen, and Lan-Da Van, “FPGA-oriented real-time EMD-based breath signal processing system on ARM11 MPCore platform,” in *Proc. IEEE International Conference on Digital Signal Processing (DSP)*, Nov. 2018, pp. 1-4, Shanghai, China.
[9] Lan-Da Van, T. C. Lu, P. Y. Chen, and H. C. Reddy, “Type-4 2-D diagonal and four-fold rotational symmetry digital filter architectures,” in *Proc. IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Oct. 2018, pp. 115-118, Chengdo, China.
[10] Z. Z. Wu, C. W. Wu, Lan-Da Van, and Y. C. Tseng, “Qnalyzer: Queuing recognition using accelerometer and Wi-Fi signals,” in *Proc. IEEE Global Communications Conference (GLOBECOM)*, Dec. 2017, pp. 1-7, Singapore.
[11] P. Y. Chen, Lan-Da Van, H. C. Reddy, and I. H. Khoo, “Type-3 2-D multimode IIR filter architecture and the corresponding symmetry filter's error analysis,” in *Proc. IEEE International Conference on ASIC*, Oct. 2017, pp. 726-729, Guiyang, China.
[12] P. Y. Chen, Lan-Da Van, I. H. Khoo, and H. C. Reddy, “New 2-D quadrantal- and diagonal-symmetry filter architectures using delta operator,” in *Proc. IEEE International Conference on ASIC*, Oct. 2017, pp. 1133-1136, Guiyang, China.
[13] P. Y. Chen, Lan-Da Van, H. C. Reddy, and I. H. Khoo, “New 2-D filter architectures with quadrantal symmetry and octagonal symmetry and their error analysis,” in *Proc. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2017, pp. 265-268, Boston, MA, USA.
[14] X. Zhang, C. W. Wu, P. Fournier-Viger, Lan-Da Van, and Y. C. Tseng, “Analyzing students' attention in class using wearable devices,” in *Proc. IEEE International Symposium on a World of Wireless, Mobile and Multimedia Networks (WoWMoM)*, Jun. 2017, pp. 1-9, Macau, China.
[15] T. H. Wu, C. H. Chang, Y. W. Lin, Lan-Da Van, and Y. B. Lin, “Intelligent plant care hydroponic box using IoTtalk,” in *Proc. IEEE International Conference on Internet of Things (iThings) and IEEE Green Computing and Communications (GreenCom) and IEEE Cyber, Physical and Social Computing (CPSCom) and IEEE Smart Data (SmartData)*, Dec. 2016, pp. 398-401, Chengdu, China.
[16] T. C. Lu, P. Y. Chen, S. W. Yeh, and Lan-Da Van, “Multiple stopping criteria and high-precision EMD architecture implementation for Hilbert-Huang transform,” in *Proc. IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Oct. 2014, pp. 200-203, Lausanne, Switzerland.
[17] J. W. Qiu, T. H. Chiang, C. C. Lo, L. M. Lin, Lan-Da Van, Y. C. Tseng, and Y. T. Ching, “Continuous human location and posture tracking by multiple depth sensors,” in *Proc. IEEE International Conference on Internet of Things (iThings), and IEEE Green Computing and Communications (GreenCom) and IEEE Cyber, Physical and Social Computing (CPSCom)*, Sep. 2014, pp. 155-160, Taipei, Taiwan. [Best Paper Award]
[18] T. C. Lu, S. H. Hsu, S. J. Tzeng, C. M. Chang, and Lan-Da Van, “Implementation of a human-centric GUI for next-generation intensive care unit,” in *Proc. IEEE International Conference on Consumer Electronics - Taiwan*, May 2014, pp. 179-180, Taipei, Taiwan.
[19] P. Y. Chen, Lan-Da Van, H. C. Reddy, and I. H. Khoo, ”Area-efficient 2-D digital filter architectures possessing diagonal and four-fold rotational symmetries,” in *Proc. International Conference on Information, Communications and Signal Processing (ICICS)*, Dec. 2013, pp. 1-5, Tainan, Taiwan.
[20] I. H. Khoo, R. C. Reddy, Lan-Da Van, and C. T. Lin, ”Design of 2-D digital filters with almost quadrantal symmetric magnitude response without 1-D separable denominator factor constraint,” in *Proc. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2013, pp. 999-1002, OH, USA.

[21] I. H. Khoo, R. C. Reddy, Lan-Da Van, and C. T. Lin, "Delta operator based 2-D VLSI filter structures without global broadcast and incorporation of the quadrantal symmetry," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2012, pp. 3190-3193, Seoul, Korea.
[22] T. C. Lu, Lan-Da Van, C. S. Lin, and C. M. Huang, "A 0.5V 1KS/s 2.5nW 8.52-ENOB 6.8fJ/conversion-step SAR ADC for biomedical applications," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2011, pp. 1-4, CA, USA.
[23] I. H. Khoo, H. C. Reddy, Lan-Da Van, and C. T. Lin, "Generalized formulation of 2-D filter structures without global broadcast for VLSI implementation," in *Proc. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2010, pp. 426-429, Seattle, WA, USA.
[24] P. Y. Chen, Lan-Da Van, H. C. Reddy, and C. T. Lin, "A new VLSI 2-D fourfold-rotational-symmetry filter architecture design," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2009, pp. 93-96, Taipei, Taiwan.
[25] I. H. Khoo, H. C. Reddy, Lan-Da Van, and C. T. Lin, "2-D digital filter architectures without global broadcast and some symmetry applications," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2009, pp. 952-955, Taipei, Taiwan.
[26] T. Y. Sheu, Lan-Da Van, T. R. Jung, C. W. Lin, and T. W. Chang, "Low complexity subdivision algorithm to approximate Phong shading using forward difference," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2009, pp. 2373-2376, Taipei, Taiwan.
[27] L. Y. Lin, H. K. Lin, C. Y. Wang, Lan-Da Van, and J. Y. Jou, "Hierarchical architecture for network-on-chip platform," in *Proc. International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, Apr. 2009, pp. 343-346, Hsinchu, Taiwan.
[28] W. C. Huang, S. H. Hung, J. F. Chung, M. H. Chang, Lan-Da Van, and C. T. Lin, "FPGA implementation of 4-channel ICA for on-line EEG signal separation," in *Proc. IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Nov. 2008, pp. 65-68, Baltimore, MD, USA.
[29] P. Y. Chen, Lan-Da Van, H. C. Reddy, and C. T. Lin, "A new VLSI 2-D diagonal-symmetry filter architecture design," in *Proc. IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Nov. 2008, pp. 320-323, Macao, China.
[30] D. Y. Wu and Lan-Da Van, "A grouped-iterative framework for MIMO detection," in *Proc. IEEE Vehicular Technology Conference (VTC)*, Sep. 2008, pp. 1-5, Calgary, BC, Canada.
[31] T. R. Jung, Lan-Da Van, T. Y. Sheu, C. W. Lin, and W. C. Fang, "Design of multi-mode depth buffer compression for 3D graphics system," in *Proc. IEEE International Conference on Multimedia and Expo (ICME)*, Jun. 2008, pp. 789-792, Hannover, Germany.
[32] C. W. Hsueh, J. F. Chung, Lan-Da Van, and C. T. Lin, "Anticipatory access pipeline design for phased cache," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2008, pp. 2342-2345, Seattle, WA, USA.
[33] C. C. Huang, S. H. Hung, J. F. Chung, Lan-Da Van, and C. T. Lin, "Front-end amplifier of low-noise and tunable BW/Gain for portable biomedical signal acquisition," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2008, pp. 2717-2720, Seattle, WA, USA.
[34] T. R. Jung, Lan-Da Van, W. C. Fang, and T. Y. Sheu, "Reconfigurable depth buffer compression design for 3D graphics system," in *Proc. International Conference on* Multimedia and Ubiquitous Engineering, Apr. 2008, pp. 470-474, Busan, Korea.
[35] C. T. Lin, L. W. Ko, K. L. Lin, B. C. Kuo, S. F. Liang, I. F. Chung, and Lan-Da Van, "Classification of driver's cognitive responses using nonparametric single-trial EEG analysis," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2007, pp. 2019-2023, New Orleans, LA, USA.
[36] C. M. Huang, K. J. Lee, C. C. Yang, W. S. Hu, S. S. Wang, J. B. Chen, C. S. Chen, Lan-Da Van, C. M. Wu, W. C. Tsai, and J. Y. Jou, "Multi-Project System-on-Chip (MP-SoC): A novel test vehicle for SoC silicon prototyping," in *Proc. IEEE International System-on-Chip Conference (SOCC), Sep.* 2006, pp. 137-140, TX, USA.

[37] Lan-Da Van, H. F. Luo, N. H. Chang, and C. M. Huang, "A cost-effective reconfigurable accelerator for platform-based SOC design," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2006, pp. 1977-1980, Island of Kos, Greece.
[38] C. T. Lin, Y. C. Yu, and Lan-Da Van, "A low-power 64-point FFT/IFFT design for IEEE 802.11a WLAN application," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2006, pp. 4523-4526, Island of Kos, Greece.
[39] Lan-Da Van, Y. C. Yu, C. M. Huang, and C. T. Lin, "Low computation cycle and high speed recursive DFT/IDFT: VLSI algorithm and architecture," in *Proc. IEEE Workshop on Signal Processing Systems (SiPS)*, Nov. 2005, pp. 579-584, Athens, Greece.
[40] H. Y. Chao, J. S. Wang, C. M. Wu, C. M. Huang, and Lan-Da Van, "High-performance low-complexity bit-plane coding scheme for MPEG-4 FGS," in *Proc. IEEE International Conference on Multimedia and Expo (ICME)*, Jul. 2005, Amsterdam, Netherlands.
[41] Y. C. Fan, Lan-Da Van, C. M. Huang, and H. W. Tsao, "Hardware-efficient architecture design of wavelet-based adaptive visible watermarking," in *Proc. IEEE International Symposium on Consumer Electronics (ISCE)*, Jun. 2005, pp. 399-403, Macau, China.
[42] M. A. Song, Lan-Da Van, C. C. Yang, S. C. Chiu, and S. Y. Kuo, "A framework for the design of error-aware power-efficient fixed-width Booth multipliers," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2005, pp. 81-84, Kobe, Japan.
[43] C. A. Tsai, Y. T. Chou, Y. T. Chang, Lan-Da Van, and C. M. Huang, "ARM-based SoC prototyping platform using Aptix," in *Proc.* iCEER, Mar. 2005, Tainan, Taiwan. [Best Poster Award]
[44] M. A. Song, Lan-Da Van, T. C. Huang, and S. Y. Kuo, "A generalized methodology for low-error and area-time efficient fixed-width Booth multipliers," in *Proc. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Jul. 2004, vol. 1, pp. 9-12, Hiroshima, Japan.
[45] Lan-Da Van, H. F. Luo, C. M. Wu, W. S. Hu, C. M. Huang, and W. C. Tsai, "A high-performance area-aware DSP processor architecture for video codecs," in *Proc. IEEE International Conference on Multimedia and Expo (ICME)*, Jun. 2004, pp. 1499-1502, Taipei, Taiwan.
[46] Lan-Da Van and C. C. Yang, "High-speed area-efficient recursive DFT/IDFT architectures," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2004, vol. 3, pp. 357-360, Vancouver, BC, Canada.
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[49] Lan-Da Van and S. H. Lee, "A generalized methodology for lower-error area-efficient fixed-width multipliers," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2002, vol. 1, pp. 65-68, Phoenix-Scottsdale, AZ, USA.
[50] C. C. Tang, W. S. Lu, Lan-Da Van, and W. S. Feng, "A 2.4-GHz CMOS down-conversion doubly balanced mixer with low supply voltage," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2001, vol. 4, pp. 794-797, Sydney, NSW, Australia.
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