

A 2.4-GHz CMOS Down-Conversion Doubly Balanced Mixer with Low Supply Voltage

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ABSTRACT

A CMOS down-conversion mixer with the combination of Gilbert Cell mixer and modified low voltage design technique using LC-tank is demonstrated in this paper. The RF, LO and IF port frequencies are 2.4GHz, 2.3GHz and 100MHz, respectively. The measurement results of the proposed mixer exhibit 6.7dB of conversion gain, -18dBm of P_{1dB} compression point and -7.5dBm of IIP3 with -8dBm LO power and 1.8V supply voltage. The power consumption in mixer core is 5.94mW. This mixer was fabricated in 0.35 μ m 1P4M CMOS process and the size is 1.5 X 1.1 mm². It can provide 0.7dB conversion gain even though 1.3V supply voltage is utilized.

1. INTRODUCTION

In the past few years, with the growing popularity of mobile PCS, GPS, and wireless-LAN, the wireless communication business has become a big market. The manufacturers have to integrate system in order to reduce the size, weight, and cost of the products. Many researches have explored the characteristics of CMOS in radio frequency (RF) [1,2] such that deep sub-micron CMOS has become an attractive candidate in the applications of low-GHz frequency range. Unfortunately, many wireless products have short stand-by time or too heavy for hand-held due to their large batteries. Hence, low power consumption is the key design issue of wireless portable products.

Fig. 1 shows the typical front-end building blocks of a superhetrodyne receiver. Because the characteristics of image rejection filter significantly depend on output loading, the input impedance of RF port should match well to the output impedance of the image rejection filter. In order to reduce the noise figure (NF) of the overall system, the mixer should have low NF and adequate conversion gain to minimize the noise contribution of the IF stage. On the other hand, the conversion gain should not be too large because a strong signal may saturate the output of the mixer and reduce its power gain. The input 1dB

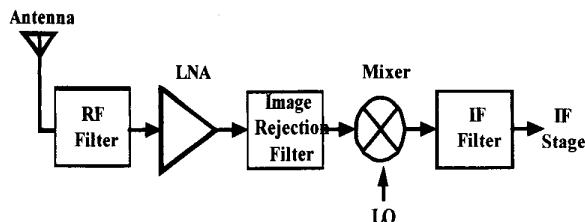


Figure 1 The RF front-end of the superhetrodyne receiver.

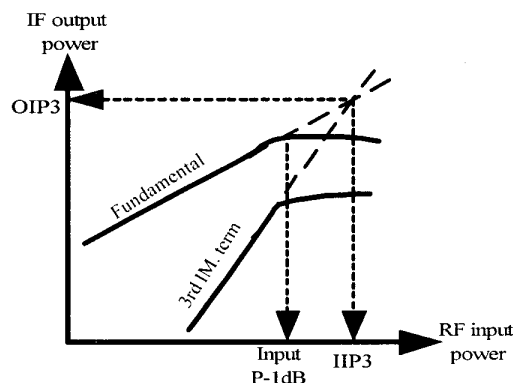


Figure 2 The definitions of input P-1dB, IIP3 and OIP3.

compression point (P_{-1dB}) measures the input power level that causes the output power deviate from its linear magnitude response by 1dB. Also the third-order inter-modulation (IM3) product generated by two undesired adjacent channel signals characterizes another parameter of mixer linearity, called third-order intercept point (IP3). The definitions of the input P_{-1dB} , input third-order intercept point (IIP3) and output third-order intercept point (OIP3) are illustrated in Fig. 2. The mixer is desired to have higher linearity, so higher input P-1dB and IIP3 are preferred.

In terms of conversion gain, mixers can be divided into two types, which are passive and active. The advantage of the passive mixers is better linearity, but the disadvantages are conversion loss, higher NF and larger LO power. In contrast to the passive mixers, the active mixers provide conversion gain, lower NF and demand smaller LO power. A smaller LO power requirement is very important in mixer design. There are several reasons. First, it is difficult to generate large LO power in low voltage and low power design. Second, larger LO power means larger LO-to-RF feed-through, which results in LO signal leaks through the antenna and becomes a strong interference to other RF systems. Third, reducing the required LO power also indicates that improve the LO-RF and LO-IF isolation.

2. CMOS Mixer Design

2.1 Gilbert Cell Mixer

Fig. 3 is the conventional doubly balanced CMOS Gilbert Cell mixer [3]. The transconductance stage consists of M1 and M2, and current commuting stage consists of M3, M4, M5 and M6.

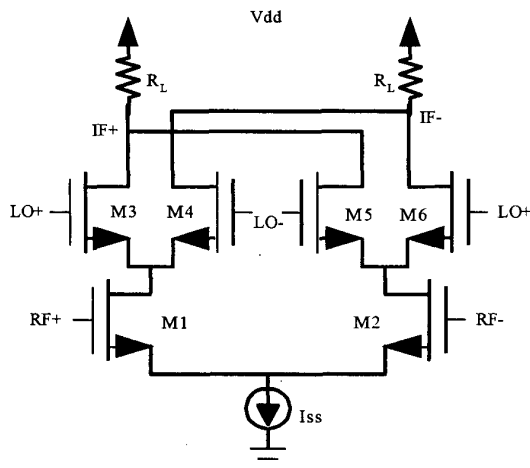


Figure 3 The simplified CMOS Gilbert Cell mixer.

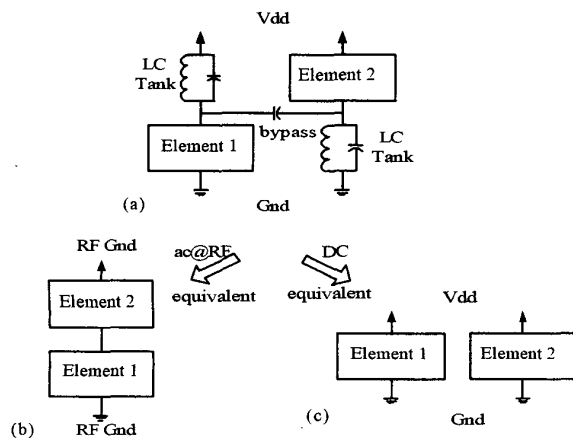


Figure 4 The low voltage topology using LC tanks and bypass capacitor (a) the complete topology, (b) RF equivalent circuit, and (c) DC equivalent current.

R_L is the load resistor. The voltage gain (A_v), which is given by Eq. 1, is determined by the transconductance of M1.

$$A_v = g_m R_L \frac{2}{\pi} \dots \dots \dots$$

Since all transistors operate in saturation region, the expected drain to source voltage is $V_T + 200\text{mV}$, neglecting body effect. For a typical V_T of 0.7V, this traditional Gilbert Cell mixer needs at least 2.7V supply voltage to operate.

2.2 Low Voltage Architecture with LC Tanks

A low voltage design technique for RF IC was proposed in [4], and Fig. 4 shows this concept. It consists of two LC tanks and one bypass capacitor. The two LC tanks resonate at the desired RF frequency to provide an infinite impedance ideally.

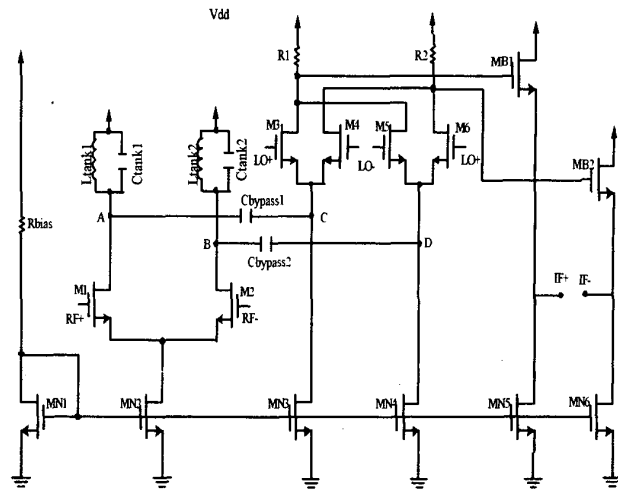


Figure 5 The simplified schematic of the proposed mixer.

The bypass capacitor is responsible for coupling the RF signal between two branches. At DC, the LC tank requires no voltage headroom, and there is only one element between supply voltage and ground in each branch.

2.3 Proposed CMOS Mixer

The proposed CMOS mixer is shown in Fig. 5. The quality factor (Q) of on-chip spiral inductor is very low (<5) due to the CMOS lossy substrate. Assume R_s is the parasitic resistor of the inductor, the equivalent resistance of the LC tank at resonance, which denoted as R_r , is given by Eq. 2.

$$R_r = R_s(1 + Q^2) \dots \dots \dots (2)$$

ASITIC [5] is used to design and simulate the on-chip inductors. If L is chosen to be 4nH, the quality factor is about 4 and the parasitic resistor is 100ohm in this 0.35um CMOS process. From Eq. 2, the R_r is calculated to be about 1700ohm. This result shows the equivalent impedance of LC tank at parallel resonance is not infinite due to the low quality factor of the on-chip inductor. If we directly apply the LC tanks to Gilbert Cell mixer, there should four LC tanks. However, the output resistance of MN3 and MN4 are about 2.5Kohm in this circuit and much larger than 1700ohm. So, MN3 and MN4 are used to replace the two LC tanks, which one is connected from node C to ground and the other is connected from node D to ground. Thus the mixer still works properly with smaller chip area. The MB1 and MB2 are added as buffers for measurement to drive 500ohm.

As compared the Gilbert Cell mixer with the proposed mixer, the first advantage of the proposed mixer is the reduction of the stacked transistors. That means it is more suitable for low voltage application than traditional Gilbert Cell mixer.

As shown in Fig. 3, the larger bias current is needed to improve the conversion gain. The larger bias current causes the larger voltage drop on R_1 and R_2 , and thus decrease the voltage headroom of the

remaining stacked MOSFETs and degrade the linearity of the mixer. Another advantage of the proposed mixer is to allow the designer to easily adjust the bias current in the transconductance stage without affecting the current-commutating stage. This is a particular important improvement in the mixer design.

The transconductances of M1 and M2 are set to 13mS. The overdrive voltages, ($V_{GS}-V_T$), of M3 to M6 are all about 70mV to reduce the required LO power and make sure M3 to M6 switch between saturation and cutoff region.

3. Simulation and Measurement Results

3.1 MOSFET Model and Simulation

There are many parasitic effects in RF design and the original model provided by foundry is not accuracy enough in such high frequency. The modified MOSFET model [6] is used to simulate the circuit. The bias range of this model is 0~3V of V_{DS} and 0~2V of V_{GS} . The frequency range is from 50MHz to 20.05GHz.

Sweep the LO power from -30dBm to +3dBm to find out the conversion gain and the required LO power. The RF input signal power is set to be -47dBm at 2.4GHz. The conversion gain is about 7.6dB when LO power is -8dBm. To ensure the mixer still provides the conversion gain when process deviation occurs, the other process corners are also used to simulate the same circuit. The result is shown in Fig. 6.

3.2 Measurement Setup and Results

The die is mounted on FR4 board for testing. The first step is to measure the S-parameters of the RF ports for designing the matching networks. After matching is completed, the test signal is differentially fed into RF and LO ports. The 180-degree lumped element hybrid is designed to convert the single-ended signal to differential signal. The measured unbalance amplitude is 0.18dB at 2.3GHz and 0.16dB at 2.4GHz. The phase difference is 180.3-degree at 2.3GHz and 180.5-degree at 2.4GHz. The testing board is shown in Fig. 7.

We set the RF power to -50dBm and LO power to -8dBm on signal generators. Fig. 8 is the IF output frequency spectrum of the single tone testing. The RF signal loss of cables and 180-degree hybrid is measured together to be 2.4dB, and the loss of cable on IF port is 0.5dB. So, the measured conversion gain is 6.7dB. After sweeping the LO power from -30dBm to +8dBm, the conversion gain is measured and also shown in Fig. 6.

The reason of the difference in conversion gain between simulation and measurement results is the LO port does not match to 50ohm perfectly while LO power is lower than -10dBm.

LO power is set to -8dBm and perform sweep of RF power from -57.5dBm to -12.5dBm to measure the linearity of the proposed mixer. As shown in Fig. 9, the simulation result of input P_{1dB} is -19.5dB and the measurement result is -18dB. Fig. 10 shows the two tones testing result of the proposed mixer.

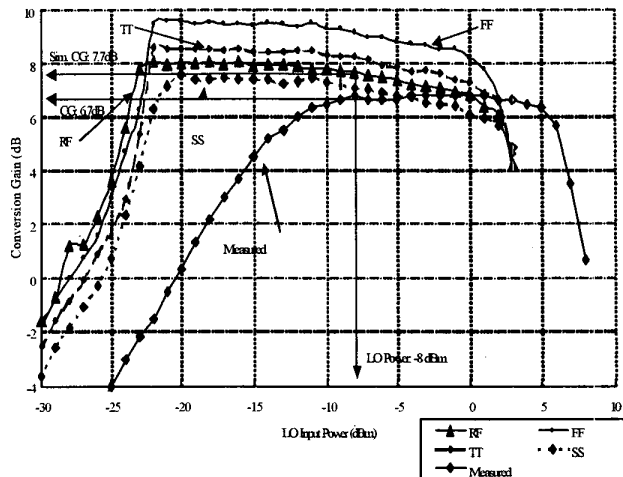


Figure 6 The simulation and measurement results of conversion gain v.s LO power of the proposed mixer.

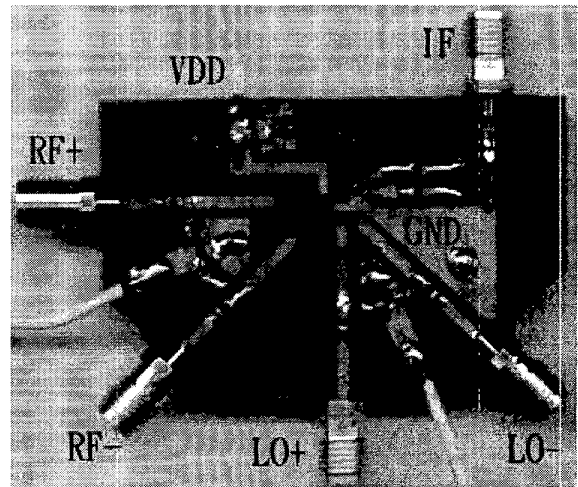


Figure 7 The test board of the proposed mixer.

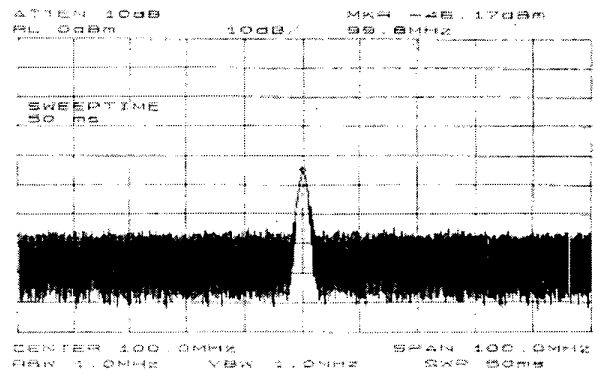


Figure 8 The IF port output frequency spectrum of single tone testing.

The RF input tones are 2400MHz and 2401MHz and LO is 2300MHz. Thus the fundamental terms of the IF output are 100MHz and 101MHz. The third-order inter-modulation terms are 99MHz and 102MHz. Fig. 11 shows the simulated and measured IIP3 results of the proposed mixer. The measured linearity is better than the simulation result because the measured conversion gain is slightly lower than the simulation result.

4. SUMMARY

The characteristics of the proposed mixer are summarized in Table 1. According to the measurement results, the proposed mixer provides 6.7dB conversion gain under the 1.8V supply voltage and it also demonstrates 0.7dB conversion gain for supply voltage as low as 1.3V. The potential for low voltage applications of the proposed mixer is proved. The proposed mixer can be easily integrated with other front-end circuits to build CMOS transceiver.

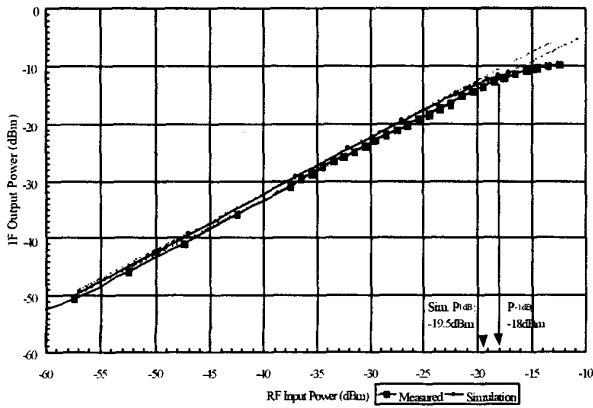


Figure 9 The simulated and measured results of P_{-1dB} of the proposed mixer.

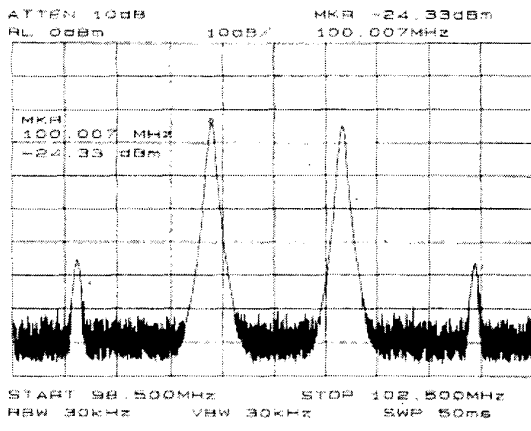


Figure 10 The IF port output frequency spectrum of two tones testing.

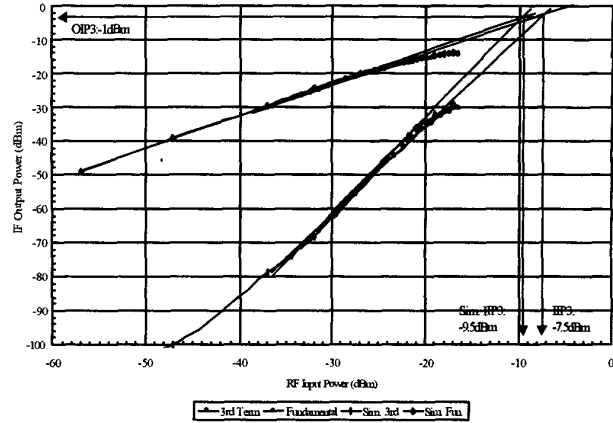


Figure 11 The simulated and measured results of IIP3 and OIP3.

Table 1 The proposed mixer performance.

RF = 2.4GHz and LO = 2.3GHz	Measured Results
LO power (dBm)	-8
Conversion gain (dB)	6.7
IIP3 (dBm)	-7.5
P_{-1dB} (dBm)	-18
Current in mixer core (mA)	3.3
Supply voltage (V)	1.8
Power consumption (mW)	5.94
Port-to-port isolation (dB)	>20
Chip size (mm X mm)	1.1 X 1.5
Process	TSMC 0.35um 1P4M

5. REFERENCES

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